herein can be implemented or performed by a machine, such as a processing unit or processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A processor can be a microprocessor, but in the alternative, the processor can be a controller, microcontroller, or state machine, combinations of the same, or the like. A processor can include electrical circuitry configured to process computer-executable instructions. In another embodiment, a processor includes an FPGA or other programmable device that performs logic operations without processing computer-executable instructions. A processor can also be implemented as a combination of computing devices, for example, a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. Although described herein primarily with respect to digital technology, a processor may also include primarily analog components. For example, some or all of the signal processing algorithms described herein may be implemented in analog circuitry or mixed analog and digital circuitry. A computing environment can include any type of computer system, including, but not limited to, a computer system based on a microprocessor, a mainframe computer, a digital signal processor, a portable computing device, a device controller, or a computational engine within an appliance, to name a few.

Conditional language such as, among others, "can," "could," "might" or "may," unless specifically stated otherwise, are understood within the context as used in general to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or steps. Thus, such conditional language is not generally intended to imply that features, elements and/or steps are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without user input or prompting, whether these features, elements and/or steps are included or are to be performed in any particular embodiment.

Disjunctive language such as the phrase "at least one of X, Y, or Z," unless specifically stated otherwise, is understood with the context as used in general to present that an item, term, etc., may be either X, Y, or Z, or any combination thereof (for example, X, Y, and/or Z). Thus, such disjunctive language is not generally intended to, and should not, imply that certain embodiments require at least one of X, at least one of Y, or at least one of Z to each be present.

Any process descriptions, elements or blocks in the flow diagrams described herein and/or depicted in the attached figures should be understood as potentially representing modules, segments, or portions of code which include one or more executable instructions for implementing specific logical functions or elements in the process. Alternate implementations are included within the scope of the embodiments described herein in which elements or functions may be deleted, executed out of order from that shown, or discussed, including substantially concurrently or in reverse order, depending on the functionality involved as would be understood by those skilled in the art.

Unless otherwise explicitly stated, articles such as "a" or "an" should generally be interpreted to include one or more described items. Accordingly, phrases such as "a device configured to" are intended to include one or more recited devices. Such one or more recited devices can also be collectively configured to carry out the stated recitations. For example, "a processor configured to carry out recitations A, B and C" can include a first processor configured to carry out recitation A working in conjunction with a second processor configured to carry out recitations B and C.

It should be emphasized that many variations and modifications may be made to the above-described embodiments, the elements of which are to be understood as being among other acceptable examples. All such modifications and variations are intended to be included herein within the scope of this disclosure.

What is claimed is:

1. A system comprising:

at least one hardware processor configured to render graphics of a game application, wherein computer-readable instructions cause the at least one hardware processor to:

render a plurality of frames per second during runtime of the game application, wherein each frame comprises a plurality of game elements within a game environment;

for each of the plurality of frames, before outputting the frame within the game application,

divide the entire frame into a plurality of pixel regions, wherein each pixel region comprises a plurality of pixels that is a subset of a total number of pixels in the frame;

for each pixel region of the plurality of pixel regions, each pixel region including one or more game elements of the plurality of game elements,

calculate a luminance for two or more pixels of the plurality of pixels in the pixel region;

select a highest luminance value associated with a first pixel in the pixel region and a lowest luminance value associated with a second pixel in the pixel region;

calculate a contrast ratio for the pixel region using the highest luminance value and the lowest luminance value;

automatically determine a threshold contrast ratio based on one or more game elements included within the pixel region and a light condition in the game environment;

determine whether the contrast ratio meets the determined threshold contrast ratio; and

provide a visual indication in the pixel region in response to a determination that the pixel region meets the threshold contrast ratio, wherein the visual indication is a change of color of each of the plurality of pixels in the pixel region to a predefined color such that each of the plurality of pixels in the pixel region is changed to the same color;

generate an updated frame comprising the plurality of pixel regions, wherein a subset of the plurality of pixel regions display the visual indication; and

output the updated frame for display in the game application.

2. The system of claim **1**, wherein the predefined color comprises a color that is not used in the frame.

3. The system of claim **1**, wherein the frame comprises at least one of a still image or a frame in a video associated with the game application.

4. The system of claim **1**, wherein to determine a pixel region in the frame, the computer-readable instructions cause the at least one hardware processor to access a size and